An Improved Boost Charge Inverter Circuit for PV Application without Static Device

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***Abstract*—**The role of renewable energy system is highly prescribed nowadays for electrification problem in the emerging world. This will satisfy the electricity production demand in rural and remote areas. This paper is focusing about the leakage occurring in the ampere ratings. The PV panel in combination with transformer based system will have the limitations like current cost and weight, to overcome this electronic transformer is proposed. The hardware prototype including the gating circuit, Electronic transformer- inverter is implemented using Boost charge pump. ***Keywords*— Ampere rating, Boost charge circuit, common mode voltage, PV Panel, Solid state transformer (SST).**

I INTRODUCTION

The purpose of this work is to generate improve the performance at low cost and reduced complexity under stable operation Solid State Transformer by reducing the leakage ampere rating. In today's world increasing of the power demand has been formulated as great issue. In order to meet out the growing demand more researches are going in renewable energy. In comparison to other sources of energy the demand will be met out easily as solar energy is widely available. The demand electricity is obtained by using solar energy and it is further used to power the domestic appliances. The losses are made higher by providing isolation between solar panel and power grid using transformer by ampere rating compensating for the economic issue due to the increased ampere current rating losses which results from presence of static transformer in PV system [1]-[6], [11],[12]. Solar technologies use the sun's energy to produce electricity and the direct current is obtained from photovoltaic panel. Photovoltaic cells are in continuous usage and the research people through their innovative methods found the different methods to improve the system efficiency.

Photovoltaic is more popular in green energy based power generation and this type is required as it reduces the changes in climatic conditions with the systems extended better durability. One more advantage with PV Panels is that it offers green and sustainable environment. This reduces the emission of Carbon dioxide and thereby limitations of photovoltaic electricity can be met out easily as it converts artificial light into electricity. The modules connected within the array suggest the amount of electricity it can generate. The electricity produce by the PV cells is enormous when directly faced by the sun which is an added advantage of such system.

A solar power system is designed to supply solar power by means of photovoltaics with arrangement of components which includes solar panels to absorb as well as convert sunlight, a solar inverter, integrated battery arrangement, cabling and a solar tracking device for optional(increases the overall performance).

The output obtained from the solar panel system varies with the temperature change, irradiance and also load conditions which is more important for Tracking of Maximum Power. The maximum power can be found with help of U-A and U-P curve characteristic which is attained from the above parameters of PV panel.

An improved boost charge inverter is implemented. By means of connecting capacitor

to the load the charge pump make control over the supply voltages changes with the help of controlled switching devices. By means of connecting capacitor to the load the charge pump make control over the supply voltages changes with the help of controlled switching devices. These charge pump circuits manipulate the voltage levels in the order of double, triple, half, invert the voltages and even fractionally multiplies or either scales the voltages in the manner of ×3/2, ×4/3, ×2/3, etc. Hence it is an efficient device used to create discrete multiples of the input voltage and the circuit produces arbitrary workable voltages with changing the modes based on the circuit design topologies and controller part. This paper proposes doubled output voltage using charge boost inverter. In H bridges inverter high voltage side is incorporated with boost charges. The capacitor is being charged with the diode at the instant the centre of half bridge becomes low. To drive the gate of the high-side FET this charge is utilized which further increases a few voltages above the supply voltage to turn the device to on state.

The size, weight and leakage current are increased due to the transformer in PV system. The PV system efficiency, weight and size are increased by eliminating the static transformer [7]-[11]. The leakage current is produced due to the presence of galvanic isolation by static transformer. The Transformer less inverter topology like H5, HERIC is shown below with block diagram of SST.

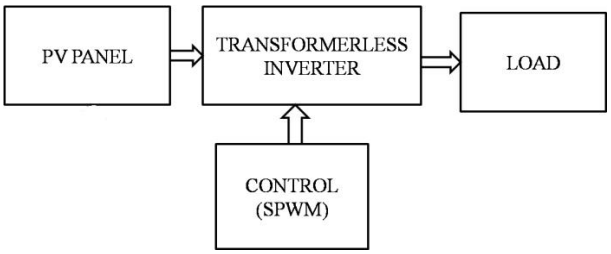


Figure 1: HERIC Inverter Topologies

II HERIC INVERTER TOPOLOGIES

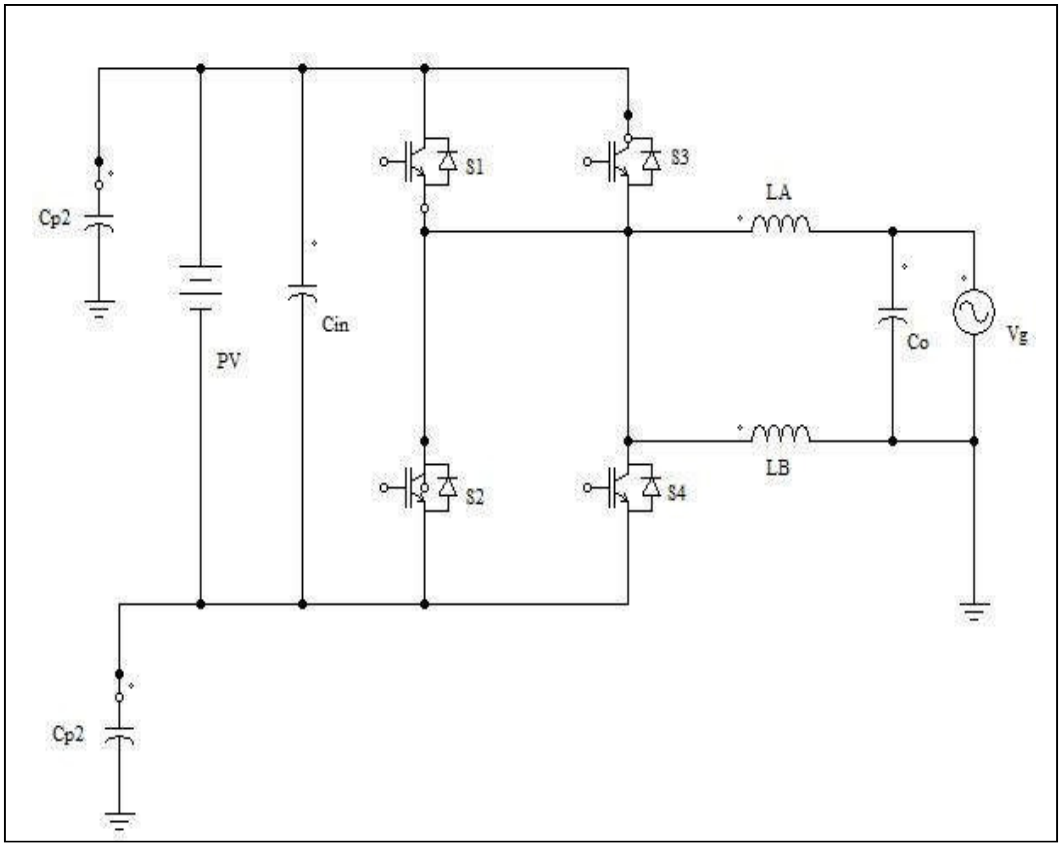
A. Review Stage

The different circuits with SST inverter are shown in Figure.2, which includes forward biased inverter that reduces the ampere ratings. The Pulse width modulation technique is used in this type of inverter. Paper imposes a better H5 inverter providing a boost converter placed in between the solar panels and the H5 inverter. Therefore circuit works under continuous conduction to make the PV panel operating with maximum power point condition in such a way the boost converters are designed. To lower the leakage current effects many end results can be viewed like conventional inverters and the complication involved is dc voltage utilization which amounts to half the percentage and hence the PV array usage should be restricted. H5 boost converter act as optimizing the impedance between the solar array and the grid so the PV is made to operate continuously with the help of H5 boost converter.

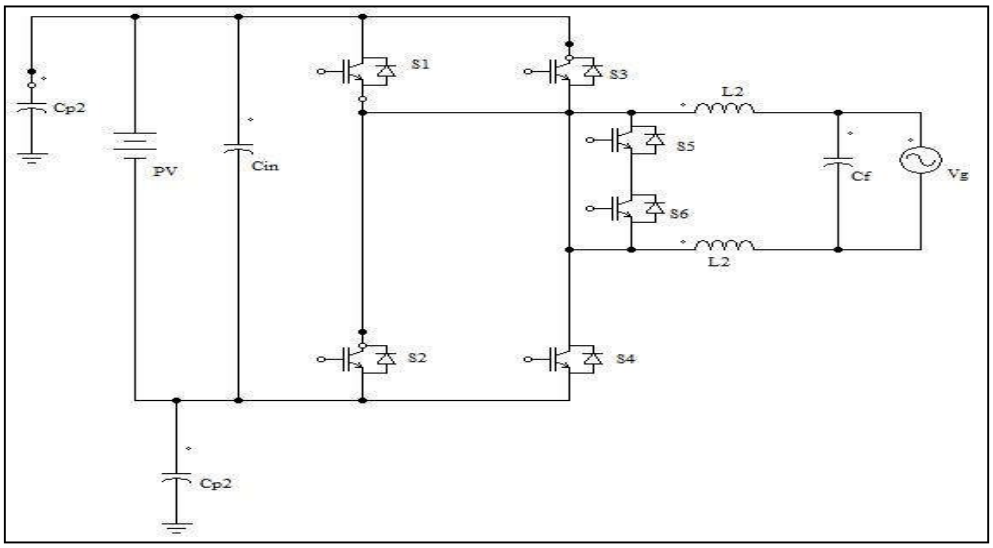
The H5 inverter has 5 switches which has an additional switch for forward biased based inverter topology. Commonly, this switch is placed near the DC side. The CM voltage is present along with small amount of leakage current. In H5 inverter three switches will on

together at once which leads to less efficient converter. The reliable inverter with high efficient circuit is shown in Figure 2(b). At a time two switches are operated same time even though the circuit consists of 6 switches. On comparison with the H5 inverter the efficiency of this inverter is high. For the purpose of decoupling, the ac side two additional switches are used. A problem with this type is its low frequency harmonic generation because the reactive power does not flow in the circuit. The grid's neutral point is fixed to PV'S negative terminal to reduce ampere ratings.

An improved Boost charge inverter circuit is analyzed in this paper. A capacitor parasitic component is kept at zero by eliminating Common mode voltage in the grid's return path that is commonly connected with the boost charge negative terminal. There is no limitation on modulation technique used in boost charge circuit which eliminates the ampere rating. The complication in the circuit is reduced by size power loss, cost and improved in power quality by using semi-conductor switches. Thus inverter power quality is improved in a better way.



(a)



(b)

Figure 2: SST circuit model (a) H5 inverter (b) HERIC inverter

III SST INVERTER AND SPWM

A. Switched Capacitor Voltage

For inverter to generate the reverse output voltage in this paper we are proposing boost charge concept. The boost charge inverter is used with 2 diodes and capacitors. Figure 3 shows the conventional H5 SST inverter topology. In this diagram, the conventional H-bridge is connected to the PV panel using the fifth change over transition control. Utility grid's frequency and the switching frequency is same as well. It removes the PV panel from the line side at zero state to disconnect the leakage ampere rating path. Hence the circuit ampere current rating is drastically reduced. During the first half cycle the upper switch group (S_1, S_3) operate alternately at the power grid's supply cycle in a second. In second half S_3 is turned on and S_1 is also on during the positive period. At supply frequency the control process produces the pure square wave.

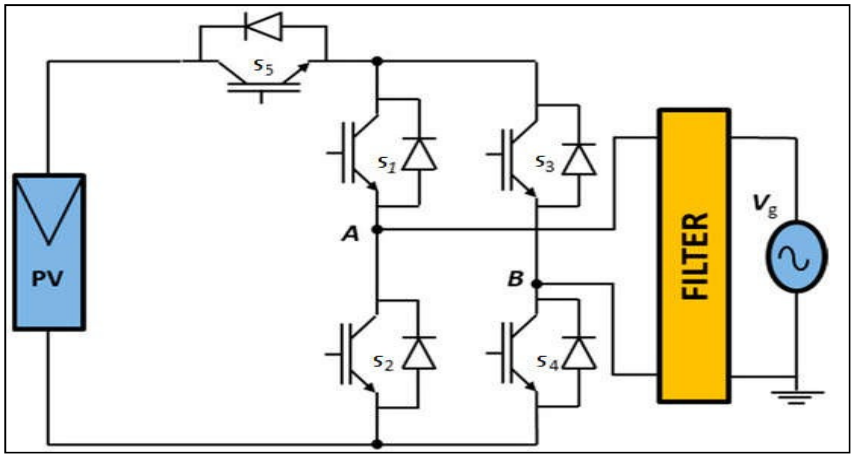


Figure 3: H5 SST inverter topology

Boost charge inverter circuit is shown in Figure 4. The circuit has 2 capacitors and

diodes. The capacitor C1is used to couple voltage point. The voltage generated at point A and C is equal in the return direct current output path. The voltages at terminal A and D are coupled using capacitor 1. The diode1 and diode2 are used to boost the output voltage. Capacitor 1 is charged using the first diode when diode D2 is forward biased. During this state the diode 1 is reversed. Capacitor 1 and 2 are charged in parallel when D1 is forward biased. At this condition the diode 2 is reversed. During the conduction period the voltages of capacitor 1 and 2 are maintained constant. By choosing perfect sequence for switching, the above mentioned conditions are obtained.

The boost charge circuit characteristics are listed below:

- Real components not present in the new methodology circuit to minimize the losses.
- By increasing the switching frequency the capacitor size is reduced.
- Ampere rating losses are reduced.
- Time period duration is decreased

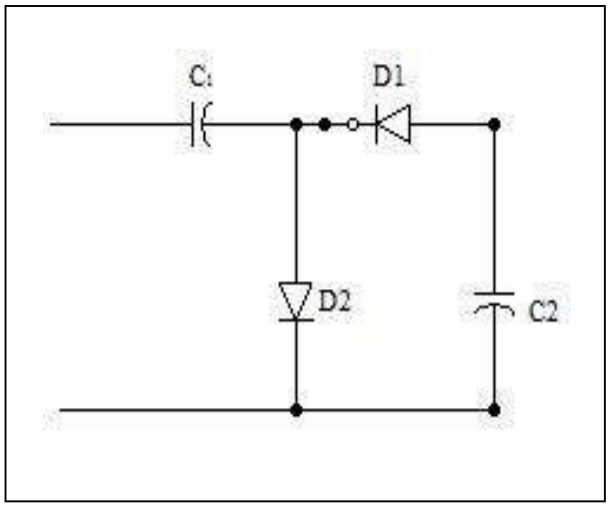


Figure 4: Charge pump circuit.

The proposed topology is shown in Figure.5.This converter has boost charger, Diodes D1 and D2, Capacitor C1 and C2 and four switching device S1, S2, S3 and S4.In the Figure 6 the values of carrier and reference wave of modulation technique which generate the pulses by Unipolar sinusoidal pulse width modulation (USPWM) for the switches in the inverter. The +V and –V are the upper and lower limit of the voltage output. +V and –V are generating during the first and second half cycles of the voltage output.

Working of the novel inverter is described in the Figure 7. In this topology 3 operating states are described in which the Figure 7 (i) and (ii) explains the first period of the supply. The zero state and positive state are present in a cycle. The switches 1 and 3 will be alternately turned ON and OFF every half cycle. Throughout this state switch 2 will remain ON. fs is the switching frequency. The S1and S2 are ON when the output voltages are equal to +V. The Figure 7 describes the +state of the inverter. Diode1 is reverse biased and the Diode 2 is forward biased during this period. The capacitor 2 voltage is kept constant. Diode

2 is used to charge the capacitor1. The Figure 7(ii) describes zero state of inverter. Diode 1 is connected parallel with the capacitor 1 and 2 during this state. The capacitor C2 is charged with -Ve polarity up to –V through C1.The boost circuit is charged using to generate the voltage. The negative voltage state is shown in the Figure 7(ii). The switch 4 and 1 is turned ON during this condition. The generated voltage in load side of the inverter is obtained across C2 when the switch 4 is turned on negatively. The capacitor C2 produces the negative voltage. By means of switch 1 and capacitor Cb, the C1 capacitor is charged to keep voltage at constant. The controls S1 & S4 are tuned on continuously. In Figure 7(ii) shows the zero state operation of first conduction which resembles the zero state operation of positive half cycle.

TABLE 1

Comparison of devices used in SST inverter topology

Inverter Type	Unipolar Device (Diode)	Power Electronic Switches	Current Path Switches
H5	**0**	**5**	**3**
HERIC	**2**	**6**	**2**
Proposed Inverter	**2**	**4**	**2**

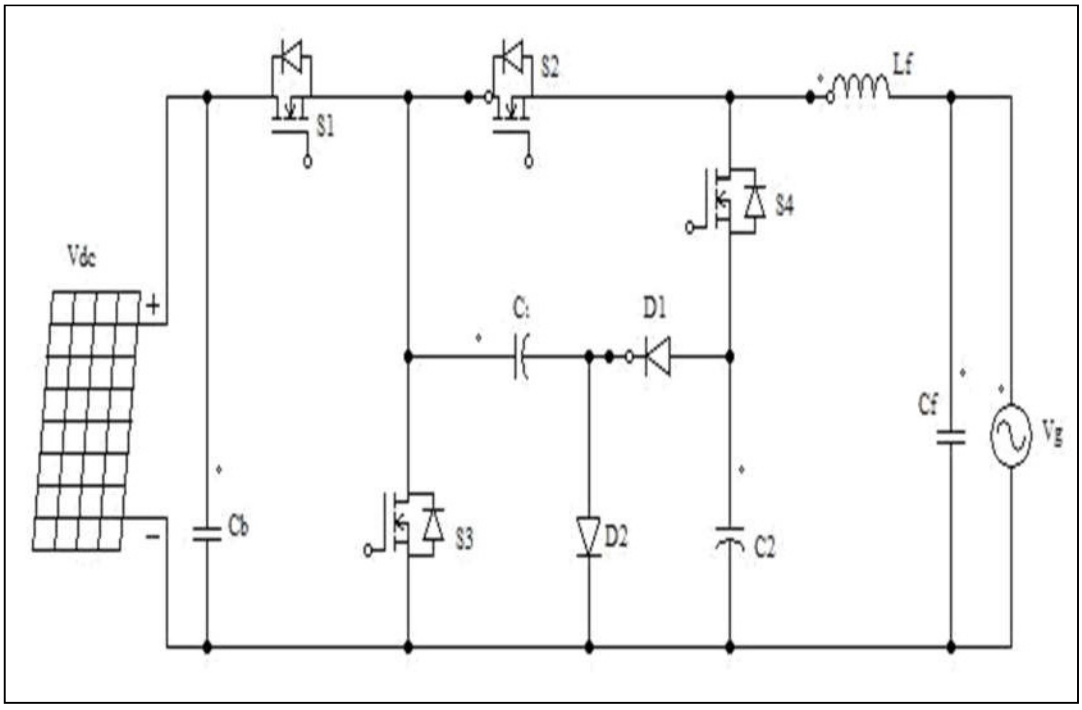


Figure 5: Proposed SST grid connected inverter

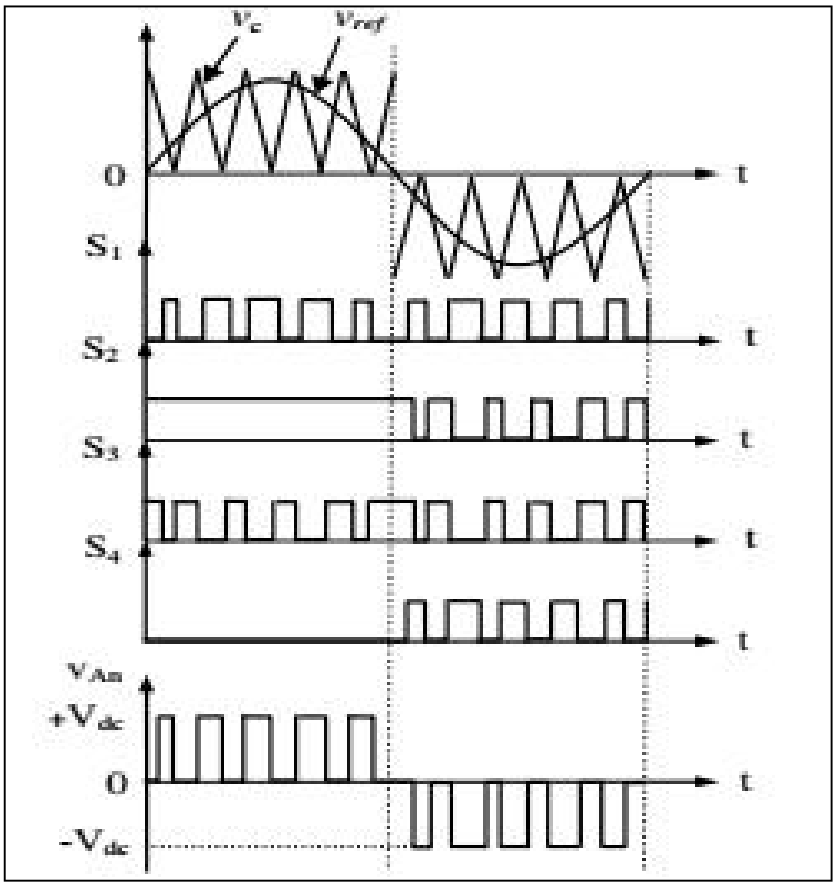
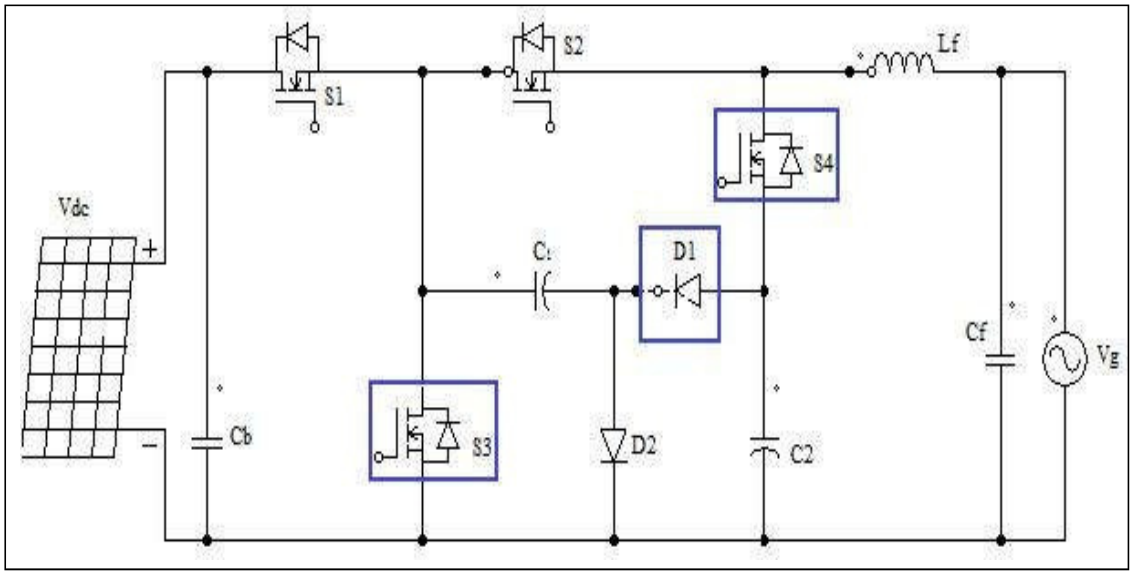
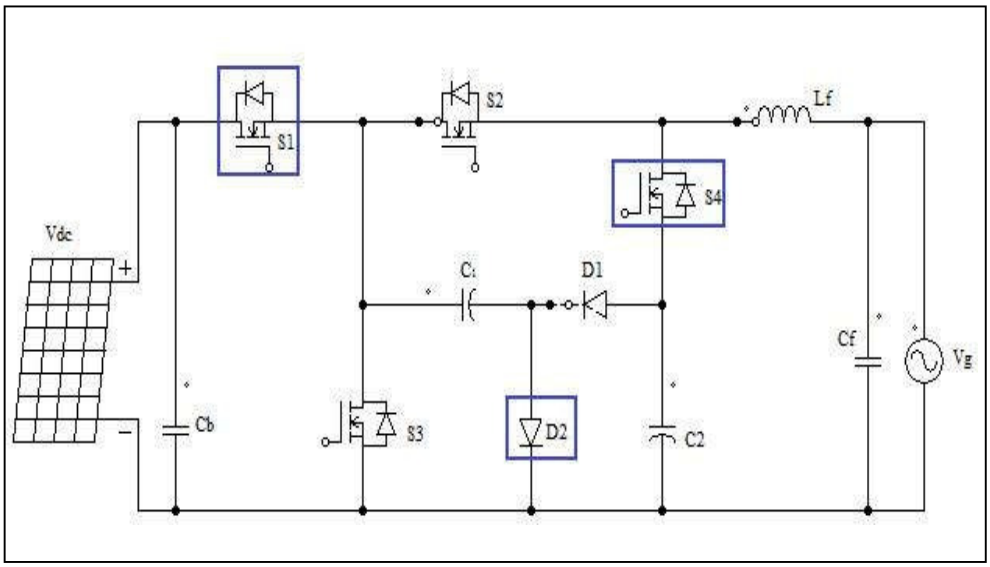


Figure 6: Unipolar SPWM method for proposed topology



(i)



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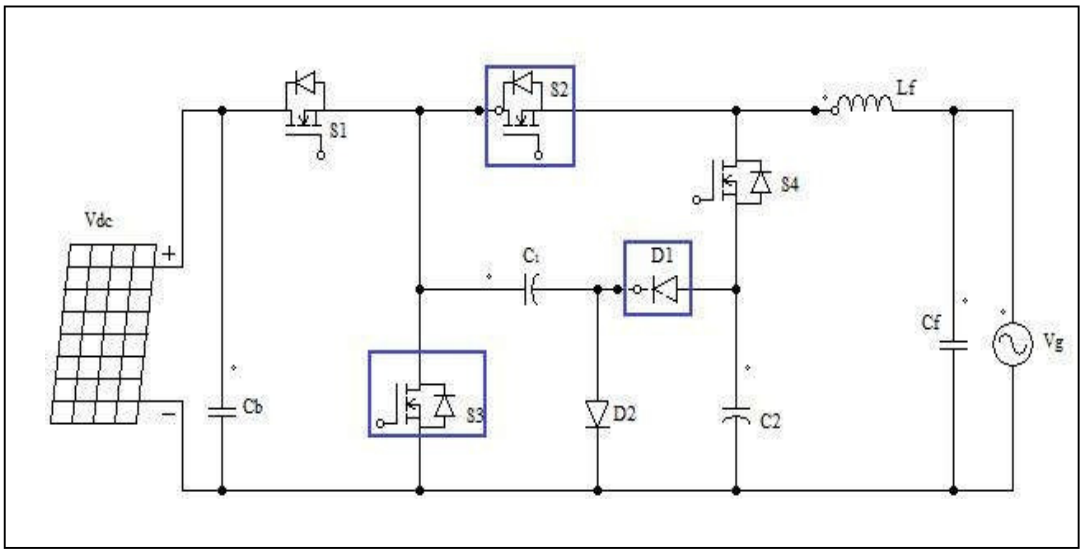

(iii)

Figure 7: Proposed SST inverter topology during (i) first half period (ii) zero state and (iii) second half period.

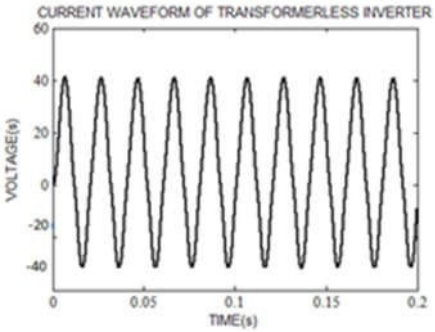

Figure 8: Current waveform of inverter topology

B. Comparison of inverter model

The proposed inverter is related between H5, HERIC in the Table 1. The passive elements used are being compared with diodes, no of switches and also with the current path switches. From this comparison it is clear that less number of components is used. Hence efficiency is improved and the ampere ratings are reduced.

IV HARDWARE IMPLEMENTATION

The proposed inverter hardware setup is shown in figure 8. The hardware prototype includes the gating circuit, inverter (without transformer) using charge pump with pulse generation using Arduino UNO and an opto-coupler. Input voltage of 24V is given to the hardware setup of single phase transformerless inverter using pump. The opto-coupler is given a supply of 5V using regulated power supply. It is seen that the program coding for sinusoidal pulse width modulation is fed to Arduino from which, Arduino output is given as the input to the opto-coupler. Figure.10. and Figure.11.describes about switching pattern of switch S1, S3 and S2, S4. The output of the opto-coupler is given to the gate of the four MOSFET switches in the circuit. When all these connections are given and the supply to the hardware is given it produces an output of 50V (pk-pk) at 50Hz frequency. Figure.12. shows the current waveform of the hardware output which is similar to the simulation result in figure 8.

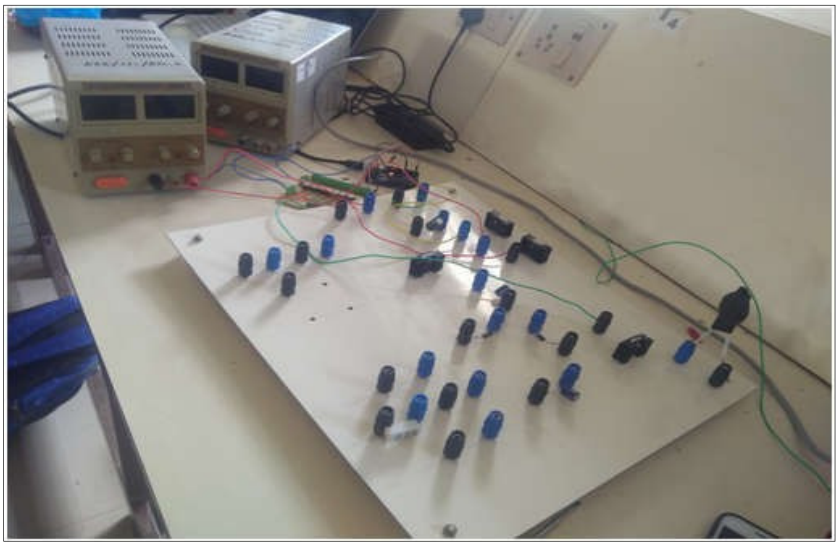

Figure 8: Proposed Inverter Setup

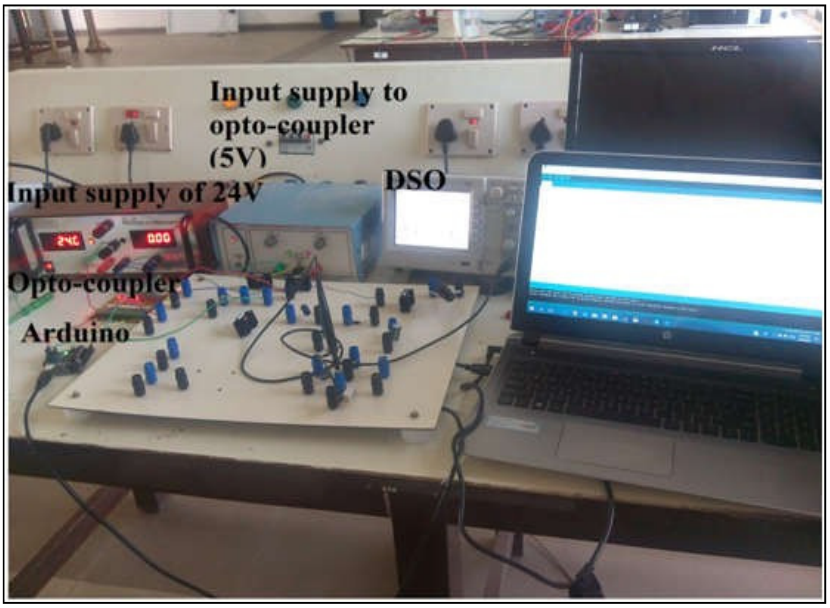

Figure 9: Full hardware setup

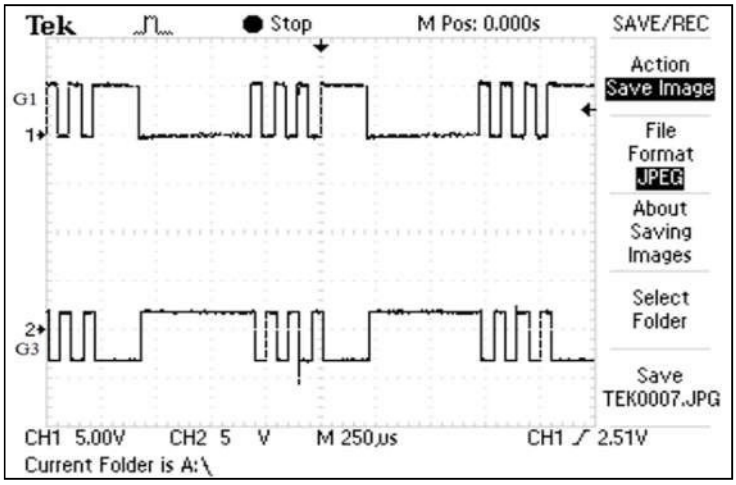

Figure 10: Gating pulse of switch S1 and S3.

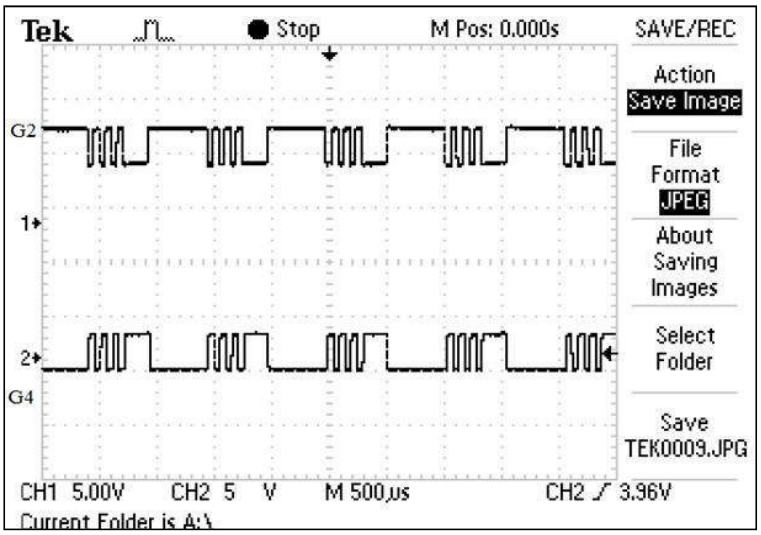

Figure 11: Gating pulse of switch S2 and S4.

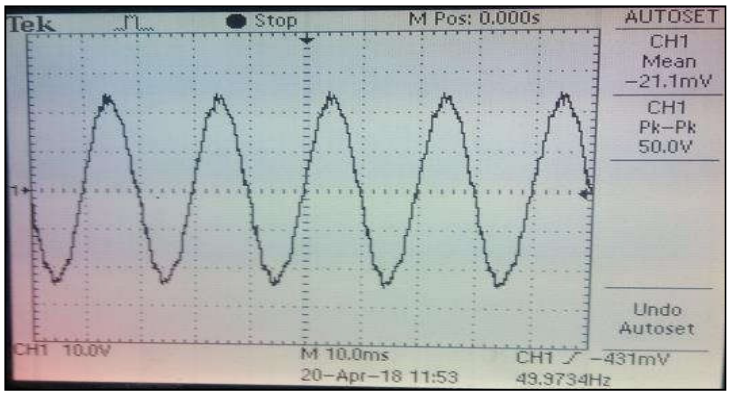

Figure 12: Hardware output of proposed inverter

TABLE 2
Inverter Specifications

Parameter	Values	Notations
Input voltage	400V	V_{dc}
Switching frequency	20 KHZ	f_s
LC filter	14mF,130µF	L_f,C_f
Capacitances	220µF,330µ	C_1,C_2

V CONCLUSION

This paper gives an elaborate idea to an improved boost charge inverter without static device. The loss due to ampere rating is lowered when the return path supply is directed to ground. By using Unipolar SPWM the topology is being modulated. Since the transformer is not present, the losses are reduced which gives a reduced size of the system. Minimum number of components is used in the proposed system in the driver circuit which leads to less number of components. The power density is increased highly because of the circuit

complexity is reduced. A nearly sinusoidal output voltage and current is obtained and the harmonic level is reduced. The novel inverter has many advantages compared with the HERIC and H5 inverter. The output voltage of 50V at 50Hz is obtained by implementing the hardware setup with SST combined with boost charge inverter.

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